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METHOD OF IMPROVING ALIGNMENT FOR SEMICONDUCTOR FABRICATION

Abstract

A method of improving alignment for the fabrication of bit line contacts (CBs) is disclosed. A substrate including a memory array area and a peripheral area is provided. A plurality of columns of word lines are laid on the substrate within the memory array area, and at least one alignment mark is provided within the peripheral area. A dielectric layer is deposited over the memory array area and peripheral area to cover the plural word lines and the alignment mark. A thin SiN film is deposited over the dielectric layer. A polysilicon hard mask layer is then deposited over the thin SiN film. A GV photoresist is formed on the polysilicon hard mask layer. The GV photoresist is subjected to suitable radiation exposure and then developed to form an opening that exposes a portion of the polysilicon hard mask layer above the alignment mark. The exposed polysilicon hard mask layer is then etched away through the opening, thereby exposing a portion of the thin SiN film within the opening.